Author: Jason Houston

# Speed Up The VR11.1 Design Process With Help From iSim:PE

## VR11.1 Voltage Regulator Design

Intersil offers a family of controllers that can be used to implement voltage regulators (VRs) that are fully compliant with Intel's VR11.1 specification. Table 1 lists the available controllers and distinguishing functionality.

VR11.1 microprocessors from Intel require a tightly regulated output voltage over a wide range of line and load variations. The design and verification process to ensure a regulator can pass the Intel specification, thus can be tedious and time consuming.

To help speed up the design and verification process a simple yet powerful model can be implemented using Intersil's iSim simulation tool. The model can be used to test load transient response, loop stability and dynamic VID transitions very quickly to get immediate feedback on component selection.

This application note will focus on generating the VR11.1 simulation model using iSim:PE and comparing dynamic performance of the simulation model and the ISL6336EVAL1Z evaluation board.

TABLE 1. VR11.1 CONTROLLERS AND FUNCTIONALITY

| PART NUMBER | MAX NUMBER OF PHASES | DIODE EMULATION | GVOT | DROOP | CPURST DELAY FUNCTION |
|---|---|---|---|---|---|
| ISL6333 | 3 | Yes | Yes | Yes | No |
| ISL6333A | 3 | No | No | Yes | No |
| ISL6333B | 3 | Yes | Yes | Yes | Yes |
| ISL6333C | 3 | No | No | Yes | Yes |
| ISL6334 | 4 | Yes | Yes | Yes | No |
| ISL6334A | 4 | No | No | Yes | No |
| ISL6334B | 4 | Yes | Yes | Yes | Yes |
| ISL6334C | 4 | No | No | Yes | Yes |
| ISL6334D | 4 | No | No | No | No |
| ISL6336 | 6 | Yes | Yes | Yes | No |
| ISL6336A | 6 | No | No | Yes | No |
| ISL6336B | 6 | Yes | Yes | Yes | Yes |

## Intersil's iSim Simulation Tool

Intersil offers an interactive web-based simulation tool called iSim for helping engineers select devices and components from Intersil's broad portfolio of high performance analog products.

For power management products many reference designs are available. These reference designs can be modified to fit custom design requirements. Reference designs for each of Intersil's VR11.1 compliant controllers are available. iSim uses the full controller and driver switching model to allow the user to characterize the transient response, loop stability, output voltage ripple, and other performance characteristics of a VR11.1 regulator design.

The full switching model provides great insight into VR performance and behavior and the simulation results can expose areas of the design that may not meet specifications and need improvement. However, the simulation time of the full switching model can be time consuming.

To reduce simulation time an averaged model of the switching devices can be implemented along with simplified behavioral models of the key controller devices that determine dynamic performance characteristics. Intersil offers a downloadable personal edition of iSim called iSim:PE. iSim:PE is a standalone simulation tool that uses the same simulation engines as the web-based iSim tool. A simplified VR11.1 model can be generated using iSim:PE.

For more information about iSim and iSim:PE please visit the iSim section of the Intersil website www.intersil.com/iSim.

## Getting Started

### Installing iSim:PE

iSim:PE can be downloaded from the Intersil website. Go to www.intersil.com/iSim. There will be a link on the screen to download the software. This link is typically on the bottom-left of the screen. Figure 1 shows a screen shot of the link.

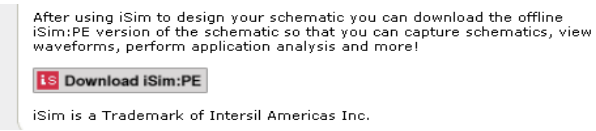


FIGURE 1. DOWNLOAD iSim:PE LINK

After clicking on the link to download iSim:PE save the executable install file to your computer hard drive (see Figure 2). When the download has completed double click on the executable file. Follow the instructions to complete the installation.

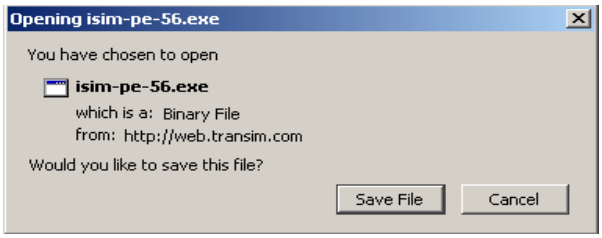


FIGURE 2. SAVE THE FILE TO COMPUTER

Once the installation has completed start the program. Select File –> New Schematic as shown in Figure 3.

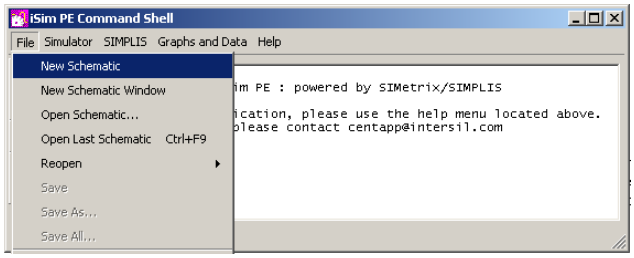


FIGURE 3. CREATE A NEW SCHEMATIC

For this model the SIMPLIS simulator engine will be used. Select File –> Select Simulator and choose SIMPLIS as shown in Figure 4.

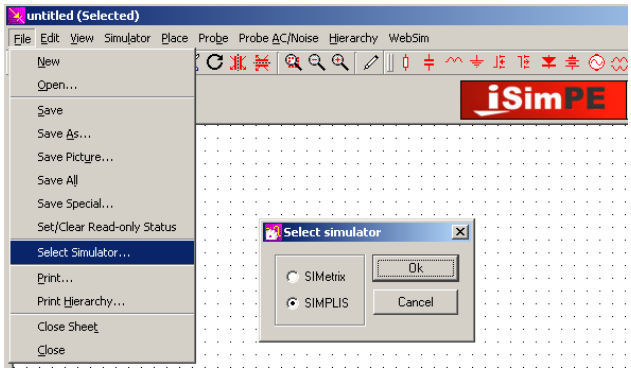


FIGURE 4. SPECIFY THE SIMULATOR ENGINE

# Generating the Model

## Multiphase Buck Regulator

Figure 5 shows a simplified 2-Phase Buck Regulator implemented with Intersil's VR11.1 control scheme. The schematic shows an error amplifier with resistor and capacitor networks for feedback compensation, two independent dual edge modulators, two power stages in parallel consisting of MOSFET drivers and synchronous buck switches, an output filter consisting of inductors and capacitors, current feedback for generating phase current and droop current information and a load modeled as an ideal current source.

The devices and components shown in Figure 5 are the key components that contribute to the dynamic response of the multiphase regulator. Each section can be simplified and modeled in iSim:PE and combined to complete the model. The following sections outline the development of the averaged model by implementing each block in Figure 5 in iSim:PE.

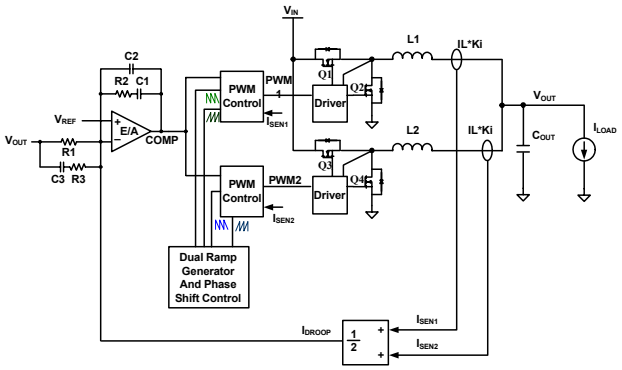


FIGURE 5. SIMPLIFIED 2-PHASE VR11.1 BUCK REGULATOR

## Output Filter and Load Generator

The output filter consists of the inductors and capacitors. The capacitors are usually a combination of bulk electrolytic or polymer capacitors and multilayer ceramic capacitors. The bulk capacitors are generally placed further away from the load than the ceramic capacitors. The output inductor can be modeled as the parallel combination of each inductor in the multiphase configuration. The load can be modeled with a current source or a resistor.

To make the design modification process easier variables can be defined for various parameters of the design. Start by placing an inductor and DCR on the schematic page. Double click on the inductor and specify the inductance value as {Lo/NA}. This will set the equivalent inductance value of the regulator to Lo (inductance per phase) divided by NA (the active number of operational phases). Place a resistor for the DCR of the inductor and set the value to {DCR/NA}.

To specify the values of the inductor variables press the F11 button on your keyboard. This brings up the iSim:PE command line window. Enter on the command line the text as shown in Figure 6.

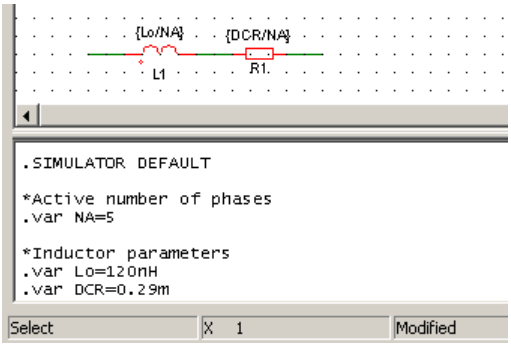


FIGURE 6. INDUCTOR MODEL

Typically there is more than one capacitor type in the output filter of a voltage regulator. Electrolytic or polymer bulk capacitors are used to supply a large amount of charge carrying capacity but are typically slower to respond to fast transients. Ceramic capacitors are used primarily to provide high speed transient support to the output voltage. Two types of capacitors can be placed in the schematic to provide design flexibility. Place two sets of capacitor models including a capacitor, inductor and resistor. You will need a variable for the number of caps per type

and the C, ESR and ESL per capacitor. Figure 7 shows an example implementation in the command line window showing the variable definitions for the bulk capacitor.

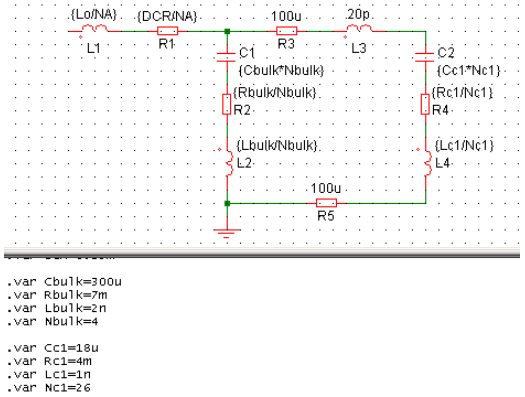


FIGURE 7. OUTPUT CAPACITOR MODEL

The load can be modeled with a current waveform generator. Place a current source waveform generator. Double click on the current source and select a pulse waveform with a 10kHz frequency and 50% duty cycle. The rise and fall time should match the slew rate specified for the application. Enter 300ns rise and fall time as a starting point. Specify a load step from 10A to 110A. Figure 8 shows the current source parameters.

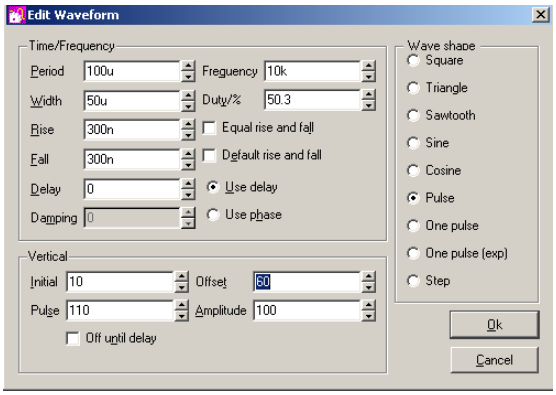


FIGURE 8. LOAD GENERATOR

The copper on the printed circuit board has some resistance and inductance. The magnitude will vary greatly depending on board layout, copper thickness and board manufacturing. Example values for PCB and load parasitic Rs and Ls for a motherboard application with a CPU socket and load are shown in Figure 9.

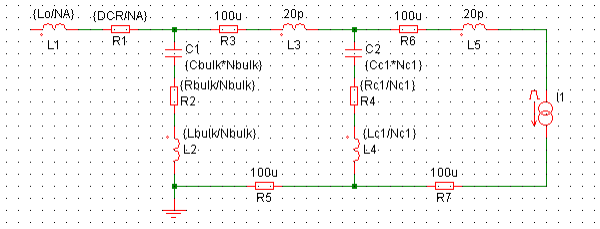


FIGURE 9. OUTPUT FILTER AND PCB MODEL

## Error Amplifier and Feedback Compensation

The error amplifier of the ISL6336 has a gain of 96dB and 80MHz bandwidth. The high performance error amplifier used on the VR11.1 controllers rarely limits the dynamic performance of the regulator. The amplifier can be modeled as an ideal amplifier with a gain of 50k. A voltage controlled voltage source with output voltage limits can be used.

The feedback compensation components can be placed in a typical configuration. Add a voltage source in series with the output of the amplifier and set it to 1.5V. Set the minimum output voltage of the amplifier to 1.3V and the maximum output voltage to 4.5V. Place a voltage source waveform generator at the positive input terminal of the amplifier. This voltage source is the reference voltage of the converter and can be used with a fixed voltage setting or a dynamic voltage to test dynamic VID transitions.

The error amplifier and feedback compensation implementation is shown in Figure 10.

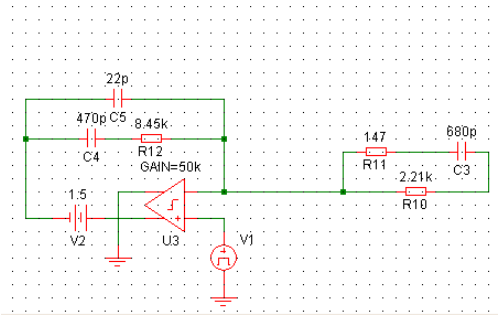


FIGURE 10. ERROR AMPLIFIER AND COMPENSATION MODEL

## Dual Edge Modulator

The VR11.1 controllers use Intersil's proprietary Active Pulse Positioning (APP) dual edge modulation scheme to improve transient performance. Both edges of the PWM output can be moved independently to provide the best response to load transients.

Figure 11 shows the output of the error amplifier (labeled COMP) as the control input to the modulator. To model the modulator the gain from the COMP input to the PWM output is considered. Figure 12 shows the change in PWM output duty cycle for a given low frequency change in COMP voltage.

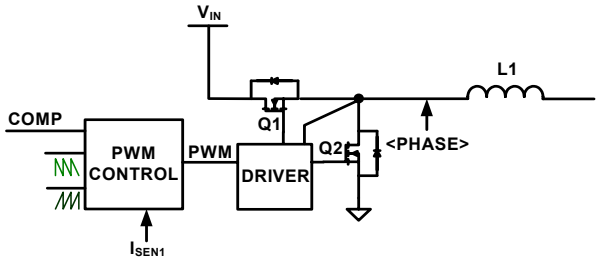


FIGURE 11. MODULATOR MODEL

There are two ramps generated in the controller to determine the pulse width. The downward sloping ramp ($D_{RAMP}$) determines the turn on edge of the PWM output and the upward sloping ramp ($U_{RAMP}$) determines the turn off edge of the PWM output. A change of 0.375V in COMP voltage leads to a 0.25 increase of PWM duty cycle. The gain from COMP to PWM therefore is 0.25/0.375V=0.67=1/1.5V. The gain from COMP to PWM is equal to $1/V_{RAMP}$ where $V_{RAMP}$ is the amplitude of the ramp input to the comparator.

Since $U_{RAMP}$ determines the on-time of the PWM the $U_{RAMP}$ amplitude is sufficient for determining $V_{RAMP}$. The slew rate for $U_{RAMP}$ is such that if the ramp continued for a full switching cycle the peak-to-peak voltage would be equal to 1.5V. Therefore the modulator gain from PWM to COMP is equal to 1/1.5V for disturbance frequencies sufficiently below the PWM switching frequency.

A more rigourous analysis of the AC modulator behavior is avoided in this application note because relatively accurate results can be obtained with the simplified results previously obtained without considering the sampling nature of the pulse width modulator.

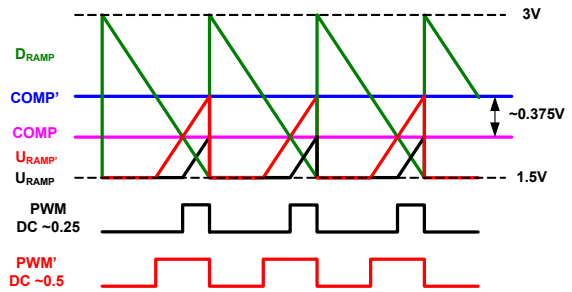


FIGURE 12. DUAL EDGE MODULATION

To remove the switches from the model the voltage at the input of the inductors can be averaged by multiplying the input voltage and the gain from COMP to PWM. For a 12V input application the gain from COMP to the input side of the inductors is 12V*1/1.5V = 8. Figure 13 shows the modulator model implemented in iSim:PE.

There is a resistance in series with the COMP input to the modulator that is used for current feedback. Set this resistor value to 2.5k.

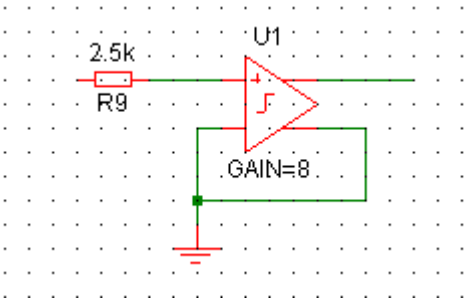


FIGURE 13. MODULATOR MODEL

## Current Sense Feedback

The VR11.1 controllers use current feedback sensed from the regulator output current for maintaining current balance between all phases in the multiphase VR, for droop control, overcurrent protection and for loop stability.

The output current is sensed mainly by detecting the voltage drop across the DCR of the phase inductors. The sensed current will be used for droop control and for loop stability in the iSim:PE model. In Figure 14 the inductor current is sensed and used for current feedback to the controller. The sensed phase currents (ISEN1/2) are summed and averaged to generate the droop current ($I_{DROOP}$). The phase current is applied to the 2.5k resistor in the modulator and the average sensed current is applied to the feedback pin to generate a droop voltage.

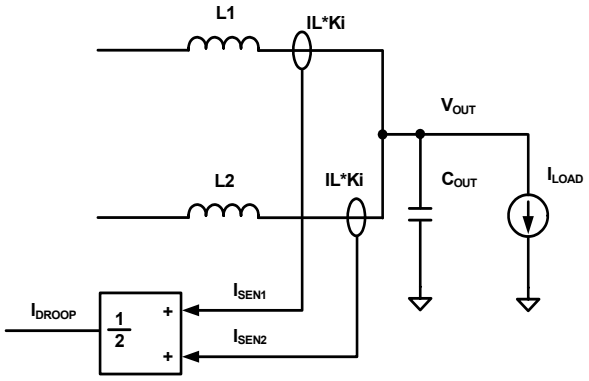


FIGURE 14. CURRENT SENSING

The current sense function can be implemented in iSim:PE according to Figure 14. Place three current controlled current sources on the schematic. The first controlled source input can be placed in series with the output inductor. Set the gain of the first source to Equation 1.

$$GAIN_{I1} = \left\{\frac{DCR}{R_S} \cdot \frac{1}{N_A}\right\} \quad \text{(EQ. 1)}$$

DCR is the resistance of the inductor, RS is the current sense resistor value, NA is the active number of operational phases. For the ISL6333 the RS resistor is internal and the value is programmed using the RSET resistor. RS for the ISL6333 is calculated as shown in Equation 2. Refer to the ISL6333 datasheet for more information.

$$RS = \frac{3}{400} \cdot RSET \quad \text{(EQ. 2)}$$

To determine NA for example, if the number of phases in the design is 5 and all phases are active NA = 5. If PSI# goes low and the controller drops all phases except phase 1 then NA = 1. The second current source input can be placed in series to ground with the output of the first current source. Set the gain to Equation 3. NPH is the total number of phases in the regulator. The output of the this current source sets the droop current. For enabling droop the output should be connected to the inverting input of the error amplifier.

$$GAIN_{I2} = \left\{\frac{N_A}{N_{PH}}\right\} \quad \text{(EQ. 3)}$$

To regenerate the phase sense current and invert the polarity connect the droop current to the input of a third current source.

Set the gain of the third current source to Equation 4. Connect the output to the modulator side of the 2.5k resistor. Refer to Figure 15 for the final circuit connections for the current sense signals.

$$GAIN_{I3} = \left\{\frac{N_{PH}}{N_A}\right\} \quad \text{(EQ. 4)}$$

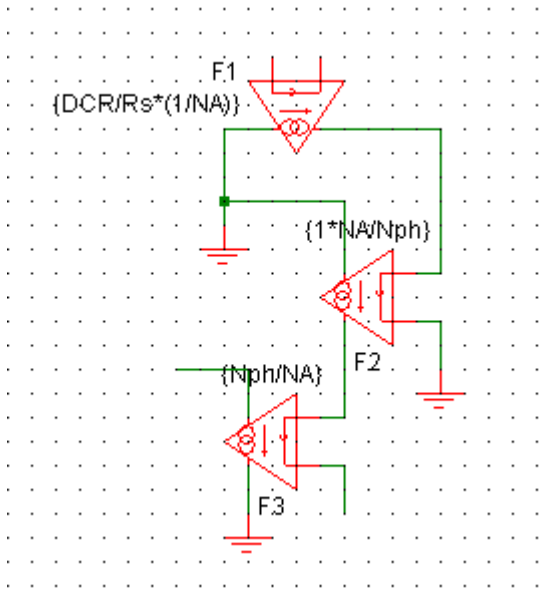


FIGURE 15. CURRENT FEEDBACK FOR MODULATION AND DROOP CONTROL

## Completing the Circuit

To complete the circuit all blocks can be combined as shown in Figure 16.

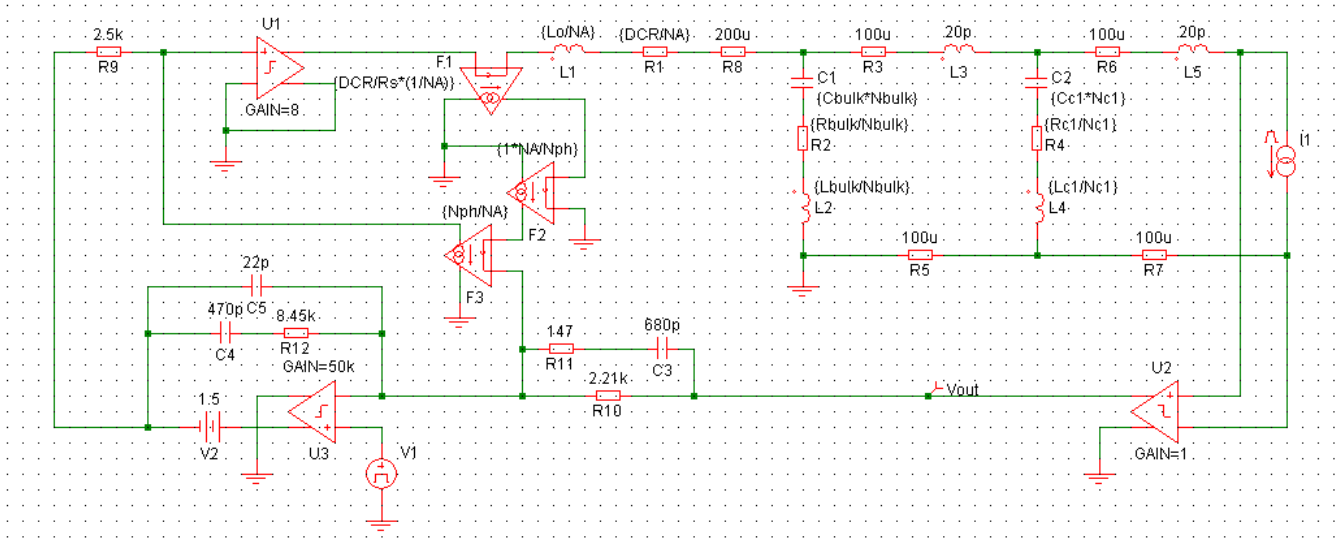


FIGURE 16. COMPLETE MODEL

# Notes On Simulation

The completed model can be used to test dynamic functionality of a regulator design and get immediate feedback on component selection and help identify aspects of the design that can be improved. The model can also be used to help get an idea about which component values can be changed and by what magnitude to help improve performance observed in hardware before physically changing any devices in the lab.

## Load Transient Response

To set up a load transient test select Simulator –> Choose Analysis in the menu on the schematic screen as shown in Figure 17.

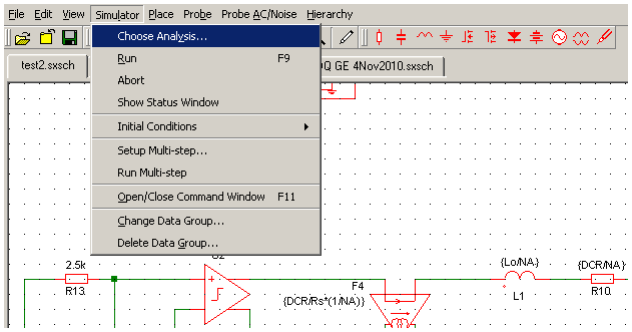


FIGURE 17. SPECIFY SIMULATION PARAMETERS

This will bring up a window where you can specify the type of simulation to run. On the right hand side under Select Analysis check Transient. Select the transient tab at the top of the window and set the Stop Time to 500µs. Under save options select All. Click ok.

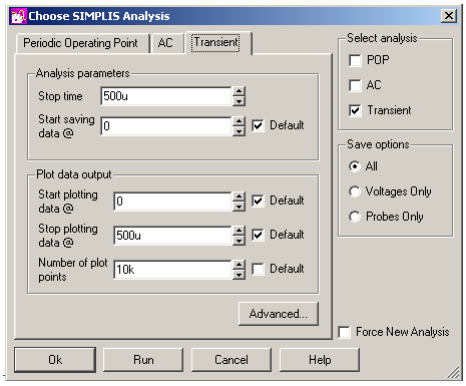


FIGURE 18. SPECIFY SIMULATION PARAMETERS

Double click on the load generator current source and make sure the parameters match what is shown in Figure 18. On the main schematic page place a current probe on the load generator current source. Place a voltage source on the output voltage. Click on Simulator –> Run. The simulation results should look similar to Figure 19.

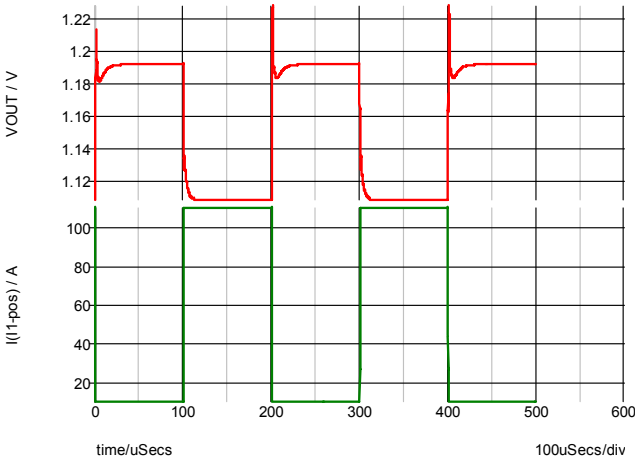


FIGURE 19. TRANSIENT RESPONSE SIMULATION

Additional simulation results can be obtained quickly and easily. Following are some example simulation results. Refer to the iSim:PE Help Menu and Tutorials for more information on how to setup and run various simulations. Figure 20 shows the command line contents for an example simulation circuit similar to Figure 16.

Figures 27 through 46 show dynamic response of the ISL6336EVAL1Z VR11.1 evaluation board compared to simulation results from the model generated in iSim:PE. The results are very similar and the simulation results match the lab test results fairly well with load frequencies approaching the PWM switching frequency.

```
.SIMULATOR SIMPLIS
.PRINT
+ ALL
.OPTIONS
+ PSP_NPT=10001
.TRAN 500u 0

.var Rs=154

.var NA=5
.var Nph=5

.var Lo=120n
.var DCR=0.29m

.var Cbulk=300u
.var Rbulk=7m
.var Lbulk=2n
.var Nbulk=4

.var Cc1=10u
.var Rc1=4m
.var Lc1=1n
.var Nc1=40

.SIMULATOR DEFAULT
```

FIGURE 20. COMMAND LINE EXAMPLE

# Additional Simulation Results

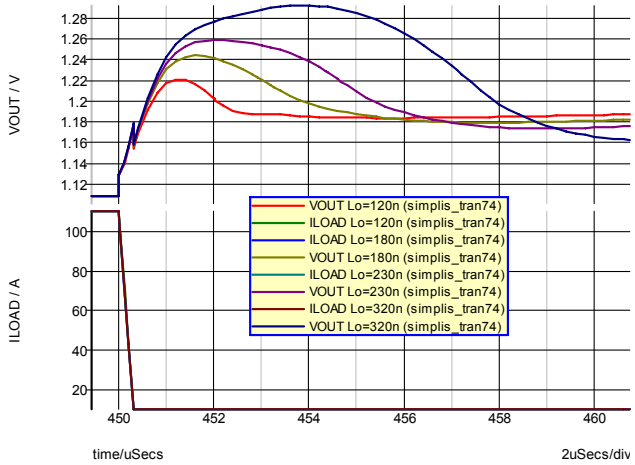


FIGURE 21. LOAD RELEASE RESPONSE vs OUTPUT INDUCTOR

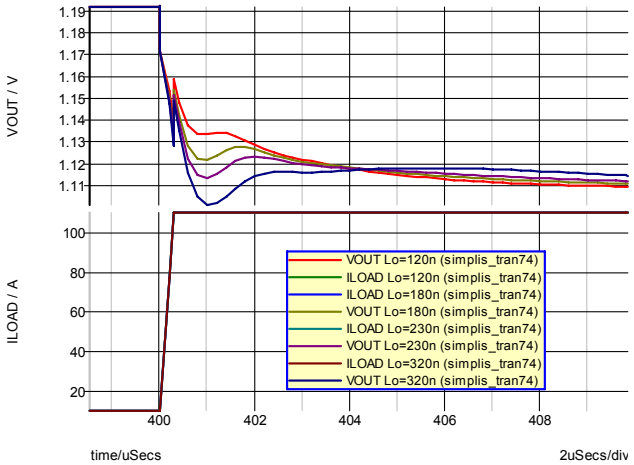


FIGURE 22. LOAD APPLY RESPONSE vs OUTPUT INDUCTOR

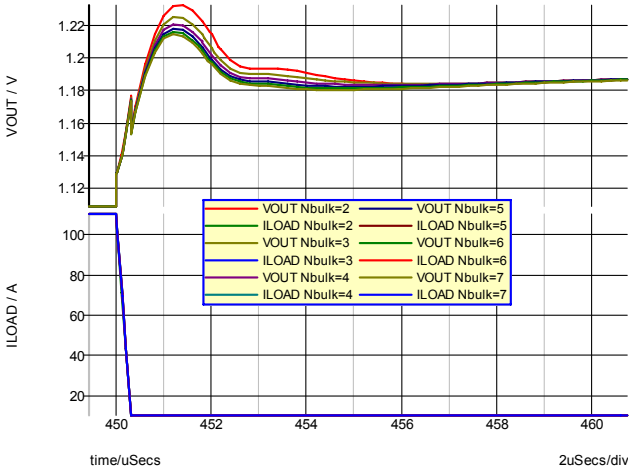


FIGURE 23. LOAD RELEASE RESPONSE vs OUTPUT CAPACITANCE

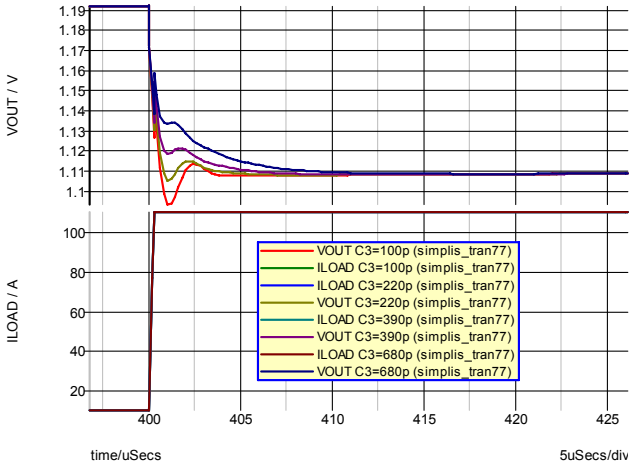


FIGURE 24. LOAD APPLY RESPONSE vs C3 CAPACITOR

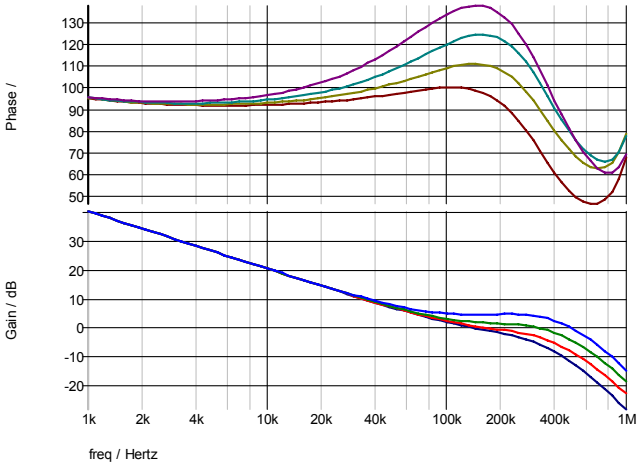


FIGURE 25. BODE PLOTS vs C3 CAPACITOR

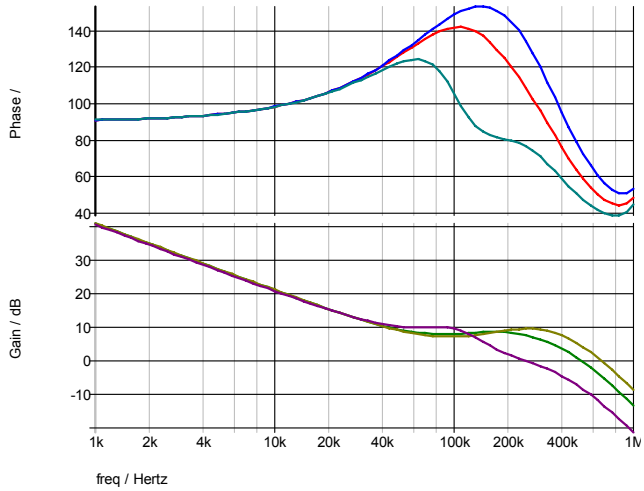


FIGURE 26. BODE PLOTS vs OUTPUT INDUCTOR

# Simulation Results Compared With Lab Test Data

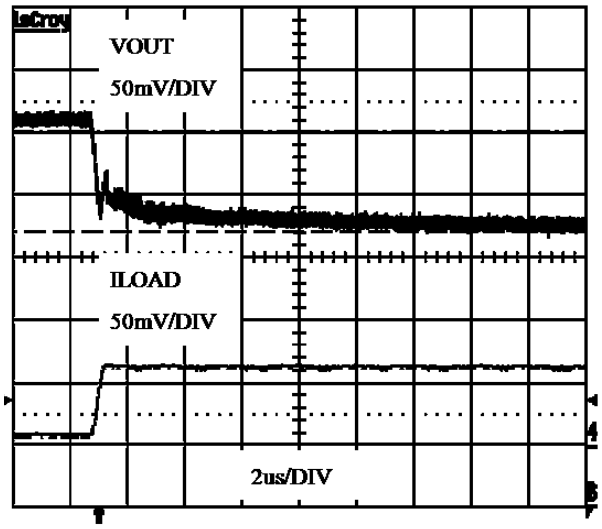


FIGURE 27. 10A TO 110A, $F_{LOAD}$ = 1kHz - ISL6336EVAL1Z

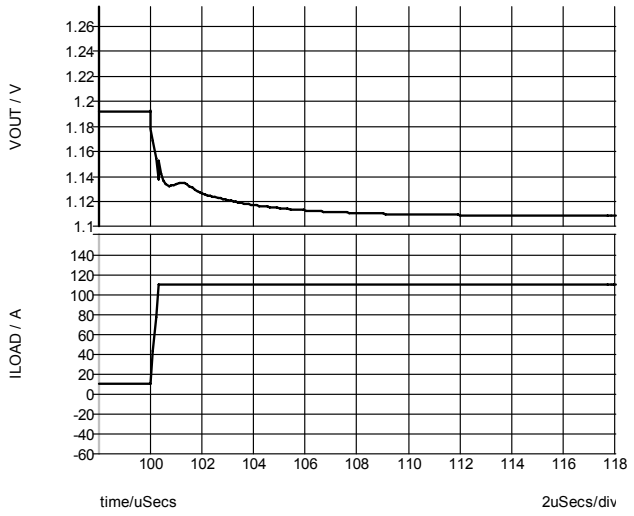


FIGURE 28. 10A TO 110A, $F_{LOAD}$ = 1kHz - iSim:PE MODEL

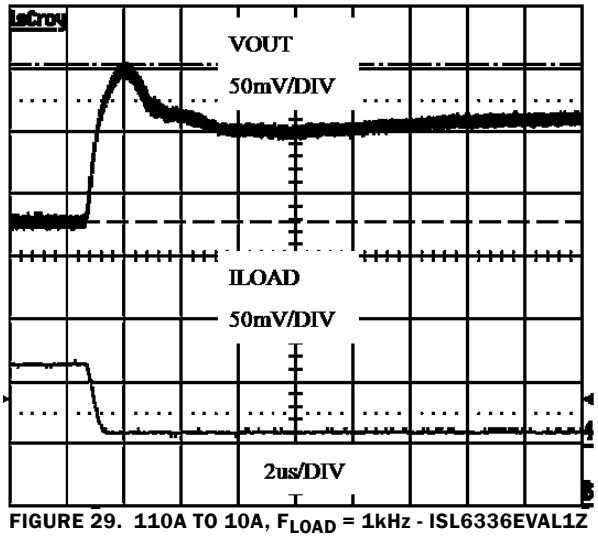


FIGURE 29. 110A TO 10A, $F_{LOAD}$ = 1kHz - ISL6336EVAL1Z

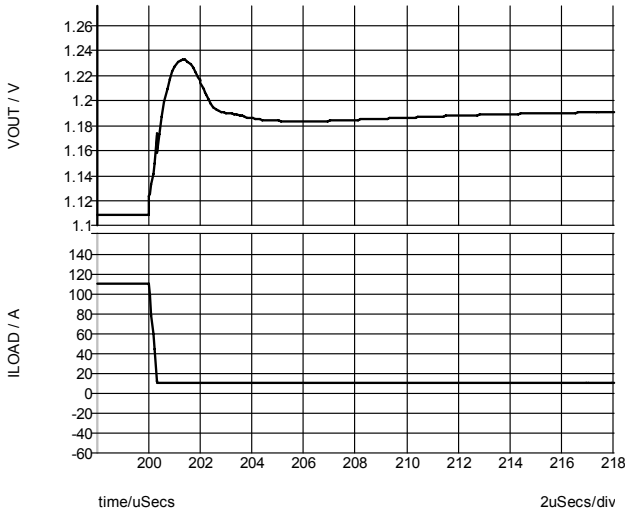


FIGURE 30. 110A TO 10A, $F_{LOAD}$ = 1kHz - iSim:PE MODEL

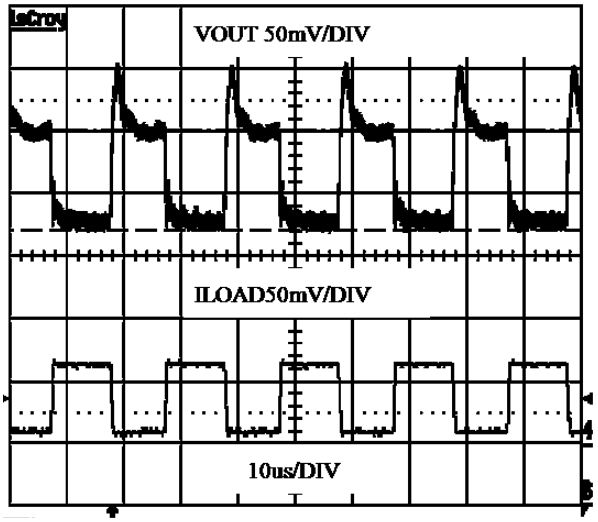


FIGURE 31. 10A TO 110A, $F_{LOAD}$ = 50kHz - ISL6336EVAL1Z

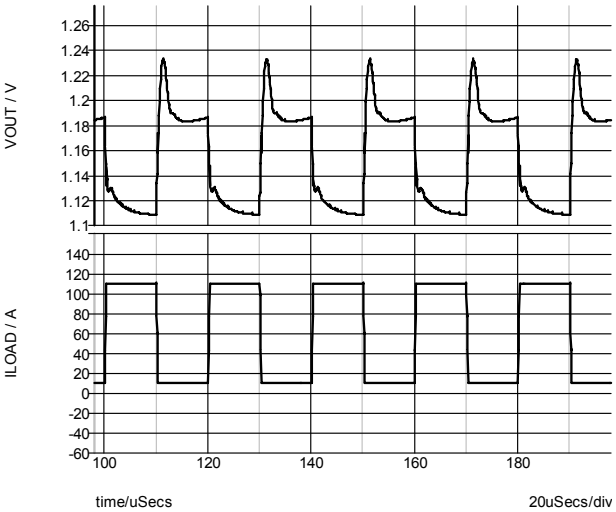


FIGURE 32. 10A TO 110A, $F_{LOAD}$ = 50kHz - iSim:PE

## Simulation Results Compared With Lab Test Data (Continued)

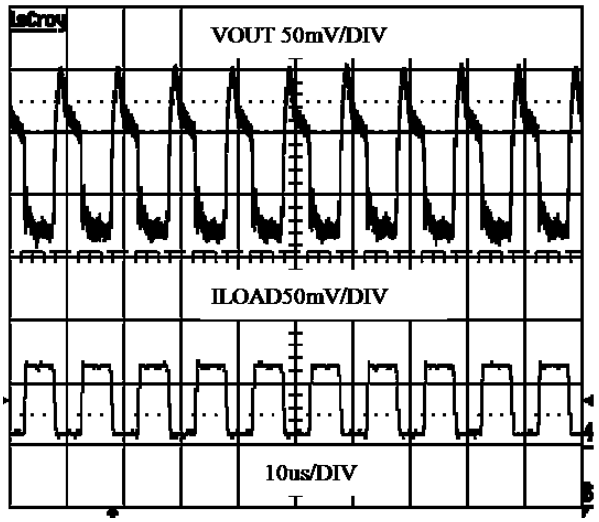


FIGURE 33. 10A TO 110A, $F_{LOAD}$ = 100kHz - ISL6336EVAL1Z

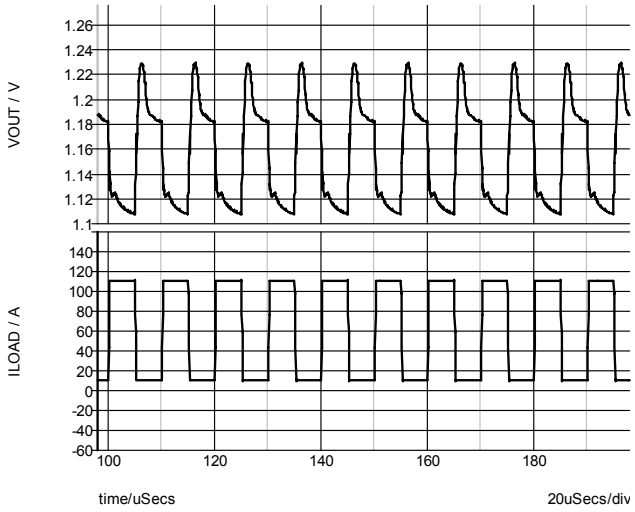


FIGURE 34. 10A TO 110A, $F_{LOAD}$ = 100kHz - iSim:PE

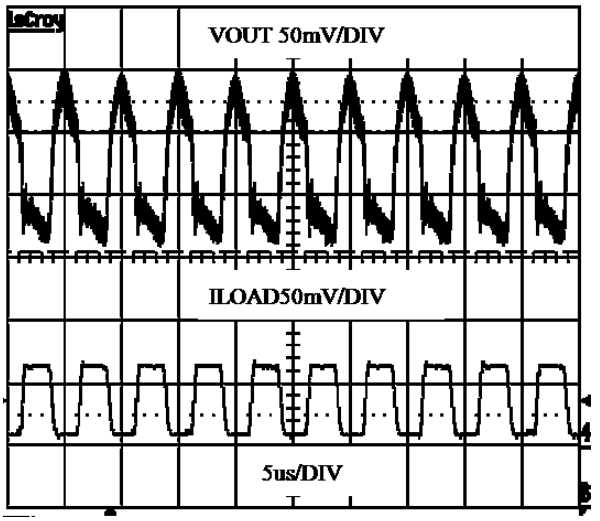


FIGURE 35. 10A TO 110A, $F_{LOAD}$ = 200kHz - ISL6336EVAL1Z

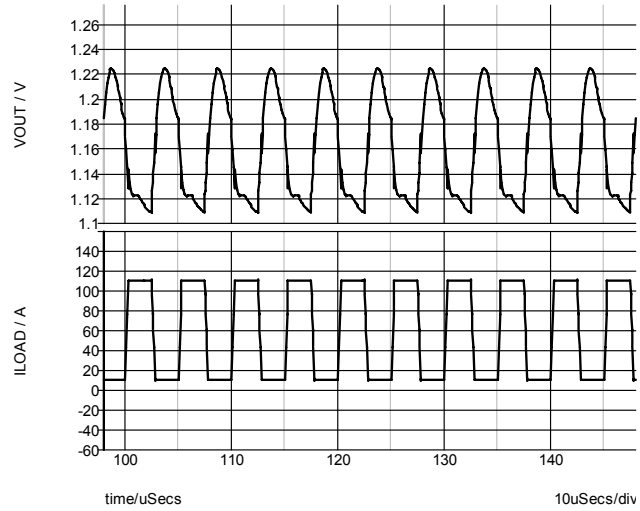


FIGURE 36. 10A TO 110A, $F_{LOAD}$ = 200kHz - iSim:PE

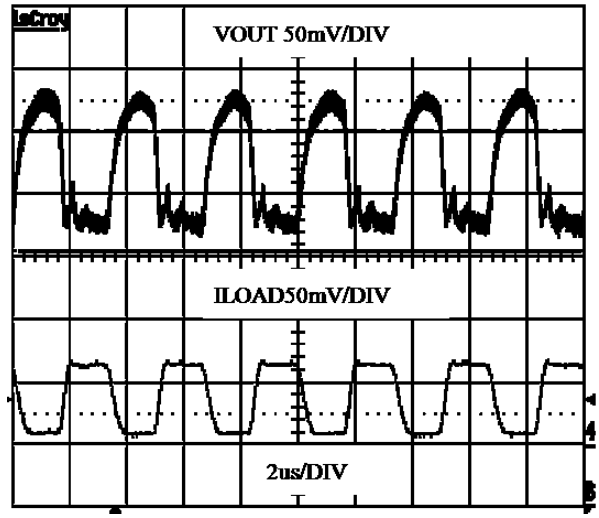


FIGURE 37. 10A TO 110A, $F_{LOAD}$ = 300kHz - ISL6336EVAL1Z

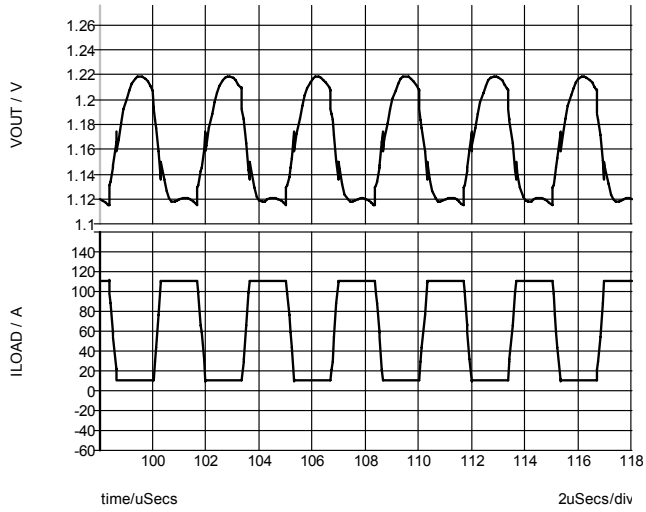


FIGURE 38. 10A TO 110A, $F_{LOAD}$ = 300kHz - iSim:PE

## Simulation Results Compared With Lab Test Data (Continued)

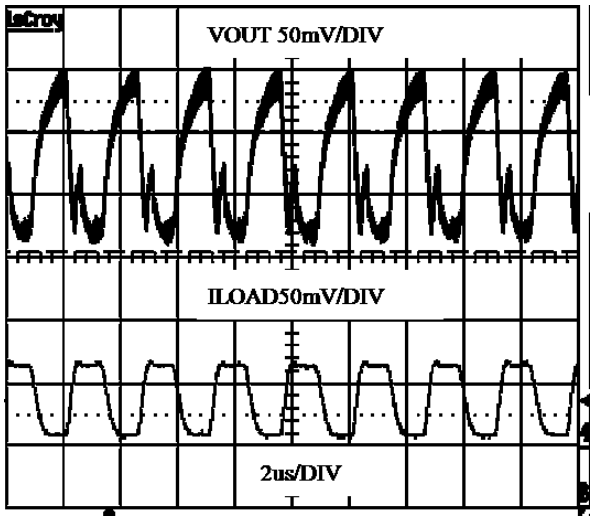


FIGURE 39. 10A TO 110A, $F_{LOAD}$ = 400kHz - ISL6336EVAL1Z

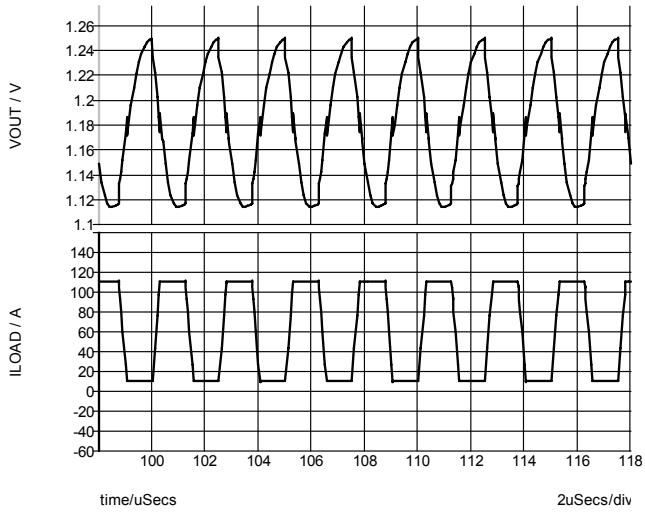


FIGURE 40. 10A TO 110A, $F_{LOAD}$ = 400kHz - iSim:PE

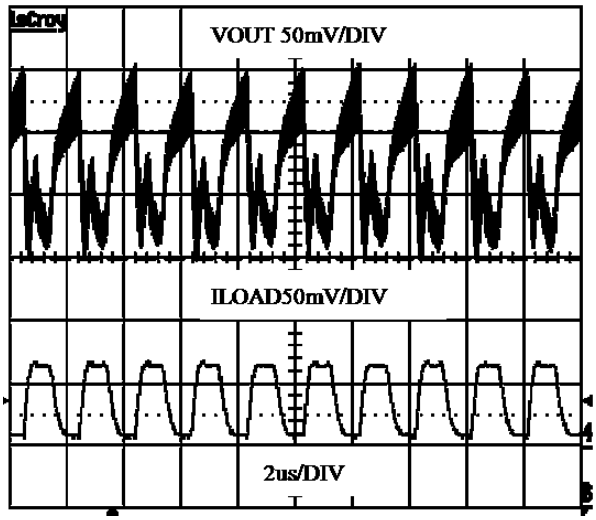


FIGURE 41. 10A TO 110A, $F_{LOAD}$ = 500kHz - ISL6336EVAL1Z

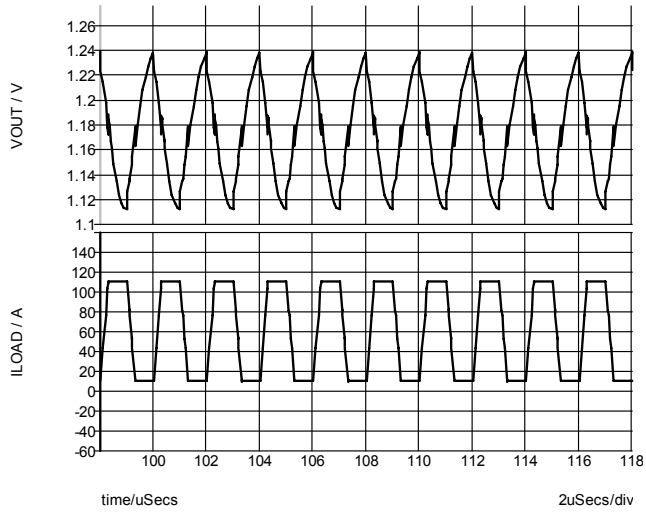


FIGURE 42. 10A TO 110A, $F_{LOAD}$ = 500kHz - iSim:PE

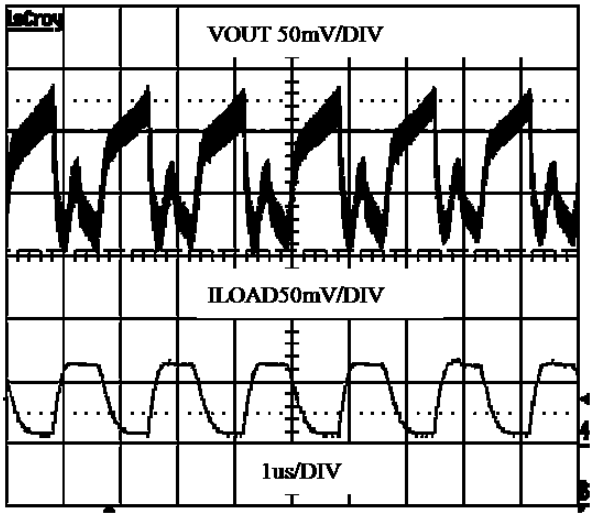


FIGURE 43. 10A TO 110A, $F_{LOAD}$ = 600kHz - ISL6336EVAL1Z

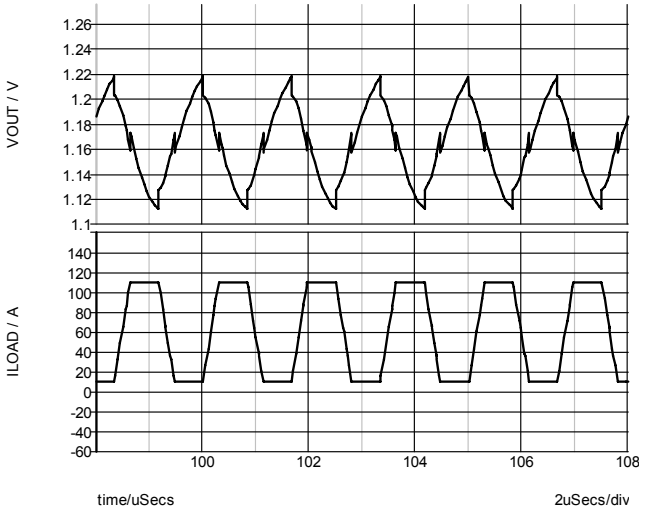


FIGURE 44. 10A TO 110A, $F_{LOAD}$ = 600kHz - iSim:PE

# Simulation Results Compared With Lab Test Data (Continued)

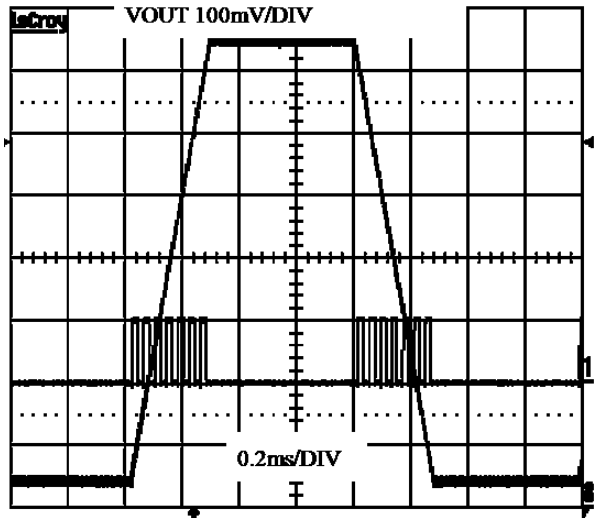


FIGURE 45. DYNAMIC VID 0.8V TO 1.5V - ISL6336EVAL1Z

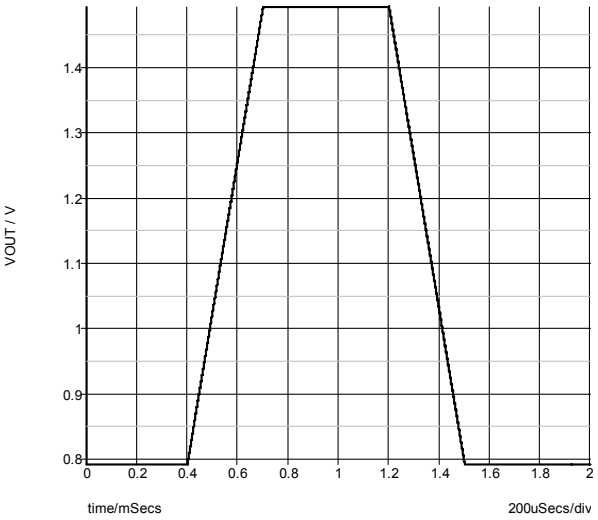


FIGURE 46. DYNAMIC VID 0.8V TO 1.5V - iSim:PE

# Summary

The simulation model generated using this application note and implemented in iSim:PE can be a useful tool to help speed up the design and troubleshooting process when designing and testing regulators using Intersil's VR11.1 controllers. For more information please visit www.intersil.com.

# References

Intersil documents are available on the web at www.intersil.com.

ISL6336 Datasheet, Intersil Corporation, FN6504

ISL6333 Datasheet, Intersil Corporation, FN6520